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Failure Mechanisms and Reliability of Low-Noise GaAs FETs

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The degradation and failure of low-noise GaAs FETs have been accelerated by various stress-aging techniques including storage at elevated temperatures with and without bias, exposure to humid atmospheres with and without bias, and temperature cycling. Several time-temperature-bias-induced catastrophic failure mechanisms have been observed, all involving the Al gate metallization. These mechanisms are Au-Al phase formation, Al electromigration, and electrolytic corrosion. Each of these processes results ultimately in an open gate. Accelerated aging also produces gradual, long-term degradation in both dc and RF characteristics, though the two are not always correlated. In fact, contrary to some expectations, contact resistance may increase almost two orders of magnitude without significant degradation in the noise figure or gain of a low-noise transistor. Besides contact resistance, other mechanisms such as traps in the channel are thought to play a role in the degradation of RF properties. It was found that all the important degradation mechanisms are bias-sensitive and that aging without bias gives erroneously long lifetime projections.

The cumulative failure distributions for the mechanisms observed approximate a log-normal relation with standard deviations between 0.6 and 1.4. The relevant degradation or failure processes have activation energies near 1.0 eV, which give rise to projected median lifetimes at 60°C (channel temperature) over 10^7 hours and corresponding failure rates (excepting infant mortality) under 40 FITs (40 per 10^9 device-hours) at 20 years of service.

I. INTRODUCTION

This paper describes the goals, experimental methods, and results of a study of the reliability of low-noise gallium arsenide field-effect transistors[1] involving about 1500 devices and 1.5 million device-hours of aging. The ultimate purpose of this work is twofold: (*i*) to calculate

the probable failure rate as a function of time; (*ii*) to identify the failure and degradation mechanisms and propose corrective action where possible. To estimate the failure rate of the device for any given operational conditions, each of these mechanisms should be characterized in terms of the nature of its cumulative failure distribution, the median life and standard deviation of the distribution, and the activation energy of the mechanism.

Since the reliability of a GaAs FET depends intimately on its structural details, especially the choice of metallization, the structure of the devices studied is described in Section II of this report. The various acceleration methods, measurement techniques, and other aspects of the experimental program will be discussed in Section III. The failure modes observed may be categorized as either sudden or gradual. The former are marked by a complete collapse of dc and RF properties and are almost always associated with a failure of the gate metallization. They are tbe subject of Section IV. (Burn-out due to undesirable voltage pulses is considered a matter of handling technique or circuit design and is not investigated in the present work.) The gradual failures involve degradation of the important RF properties, especially the noise figure and the gain. There is an associated, though not well correlated, change in the observable dc characteristics. The gradual degradation of low-noise GaAs FETs is discussed in Section V. In Section VI, the pertinent failure statistics are summarized and some cumulative failure distributions are shown. Finally, estimated failure rates under typical operational conditions are presented in Section VII, together with some prognoses with regard to other operating environments.

II. THE STRUCTURE

Two slightly different versions of low-noise GaAs FETs were studied, differing primarily in the details of the gate bonding pad. In the earlier form, shown in Fig. 1, the Al gate metallization extends under the entire bonding area which is covered by a titanium-platinum-gold final metallization.[1] In the later version, the bonding area is separated laterally from the Al to which it is connected by the Ti-Pt-Au final metal. This is shown in Fig. 2. In both cases, the gate bonding pads, as well as the source and drain bonding pads, lie on the semi-insulating substrate. A schematic cross-sectional view of the source and drain contacts is given in Fig. 3. The ohmic contact consists of a layer of 88-percent Au/12-percent Ge, topped successively by a layer each of silver and gold and then alloyed. A final metallization of Ti-Pt-Au, as described above, is applied on top of the alloyed ohmic contact.

The active n-type layer is 3000 to 6000 Å thick with a donor density of approximately 1×10^{17} cm^{-3}. An n+ layer, about 3000 Å thick and with a donor density around 2×10^{18} cm^{-3} underlies the source and drain

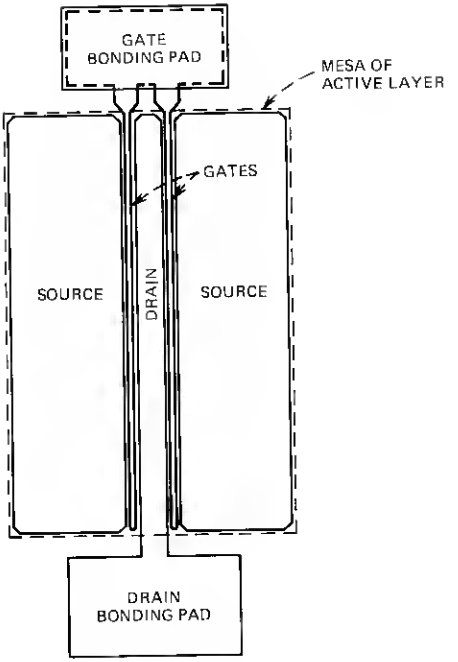

Fig. 1—Plan view of early low-noise GaAs FET.

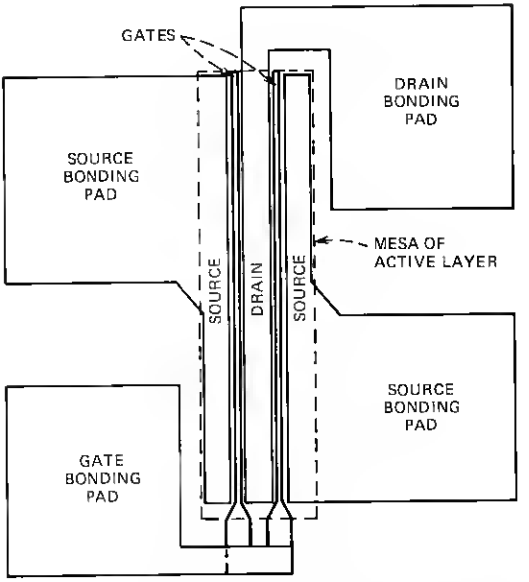

Fig. 2—Plan view of later model low-noise GaAs FET.

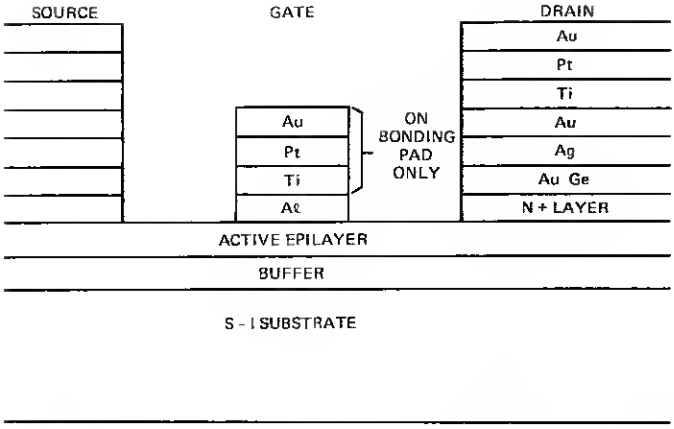

Fig. 3—Cross section of GaAs FET contact metallurgy (relative thicknesses not to scale).

contacts. A buffer layer with a donor density $< 10^{13}$ cm^{-3} and 2 to 5 μm thick separates the active layer from the semi-insulating (Cr-doped) substrate. Except in a few cases, no passivation layers were present on the finished chip. The chip size is 0.5 mm square and 50 μm thick. Each chip is bonded in a 2.5-mm square package which is hermetically sealable.

III. EXPERIMENTAL METHOD

To accelerate the degradation or failure of the GaAs FETs, a number of methods were used. The primary of these (about 1,000,000 device-hours) was aging at elevated temperatures, both with and without bias. The ambient was air at temperatures of 88°, 180°, 220°, 250°, and 275°C. The bias duplicated normal operating values consisting of 5V on the drain and a gate bias of −0.1 to −2.V, as necessary to produce 15 mA of drain current.[2] At this bias, the elevation of the channel temperature above ambient is estimated to be about 8°C. Due to the wide-band instability of GaAs FETs, RF oscillations will readily occur even at high temperatures. Such oscillations are in themselves sometimes destructive and they may also produce instantaneous, or by rectification, dc bias values of unknown and uncontrolled magnitudes. Thus considerable effort was devoted to the suppression of oscillations by various means. Dissipative media (Eccosorb), RC networks, and ferrite beads were employed, with various degrees of effectiveness. One principal difficulty was the incompatibility of some of the stabilizing components with the high temperatures involved and the fact that it is desirable to place such stabilization as near the FET as possible. Ferrite beads were the most effective and usually succeeded in quelling oscillation. Zener diodes were also employed in both the drain and gate supplies to protect the FET from destructive voltage transients.

While aging units under bias, the dc bias values could be monitored and were recorded daily. Catastrophic failures, that is, short or open circuits in the drain or gate, were thereby readily observed. RF properties could only be determined by periodic removal of the units and testing in either a tunable or a fixed-tuned amplifier. Thus, at intervals which ranged from 100 to 1000 hours, groups of FETs were temporarily removed from the aging environment and dc and RF measurements were performed. The dc characterization consisted of photographing the output characteristics from which the saturated drain current, I_{DSS}, and the low-field source-drain resistance, R_S, i.e., (dV_{DS}/dI_{DS}) at $V_G = V_{DS} = 0$, were determined. The RF parameters measured were the noise figure, NF, and the associated gain, G, at 4 GHz and 15 mA, 5V drain bias. In the case of the tunable amplifier used in the earlier stages of this study, the minimum NF was obtained; the NF obtained in the fixed-tuned amplifier (a modified Western Electric 652A[2]) was near-minimum, but not actually optimized for each device.

Another failure-acceleration technique used was storage under bias in air of 85-percent relative humidity at 85°C (referred to hereafter as 85/85). In these experiments (about 150,000 device-hours), only the gate was biased at $-4\frac{1}{2}$ or -6V with respect to the grounded drain; the source floated. Some devices were aged without bias, of course, as was also the case at the higher temperatures. The reverse leakage and the continuity of the gate were checked hourly, then daily, and finally weekly in these experiments, which varied in duration from a few hours to a year. Periodic RF measurements were generally not performed on these devices since catastrophic failure due to electrolytic corrosion of the gate was the mechanism studied. The purpose of the 85/85 experiments was to determine the integrity of "hermetically sealed" packages, the presence of corrosive contaminants therein, and the effectiveness of various waterproofing or passivation coatings.

To test the security of the thermocompression bonds of the 25-μm diameter gold leads to the source, drain, and gate bonding pads as well as to test the hermetic seal, devices were cycled, under bias and without bias, between $-40°$ and $+125°$C. The continuity of the bonds was tested before and after cycling as well as during cycling, in a few cases. Some devices were also thermal-shocked by alternate immersions in freezing and boiling water. These tests will not be discussed further, since in no case (out of 28,500 bond-cycles) was an open bond observed. In fact, no open bonds have been encountered among any of the over 1500 devices tested, before or after the various aging regimes described above. No centrifugal or vibration tests were employed in this program.

Lastly, a few lots of FETs have been aged without acceleration—that is, under normal operating dc bias (no RF) at room temperature (27°C), totaling 250,000 device-hours.

IV. CATASTROPHIC FAILURES

4.1 Au-Al phase formation

The most common cause of complete dc and RF failures encountered in this study was related to the formation of Au-Al compounds (a version of this on Si devices is known as purple plague). A dramatic example is shown in Fig. 4. In this case, the force of thermocompression bonding to the top Au layer has ruptured the integrity of the intervening Ti-Pt layer and caused contact between the Au top layer and wire and the bottom Al layer at the end of the gate structure. However, the loss of gate continuity is not due to embrittlement and subsequent parting of the bond nor to the high resistance of the Au-Al compound. Fed by the surplus of available Au, the Au-Al system (of which Au_5Al_2 is the favored end product) acts like a sink for the surrounding Al and has produced voids in the Al gate structure (the Kirkendall effect). The voids in the gate are visible in Fig. 4. The presence of Ga may catalyze this reaction

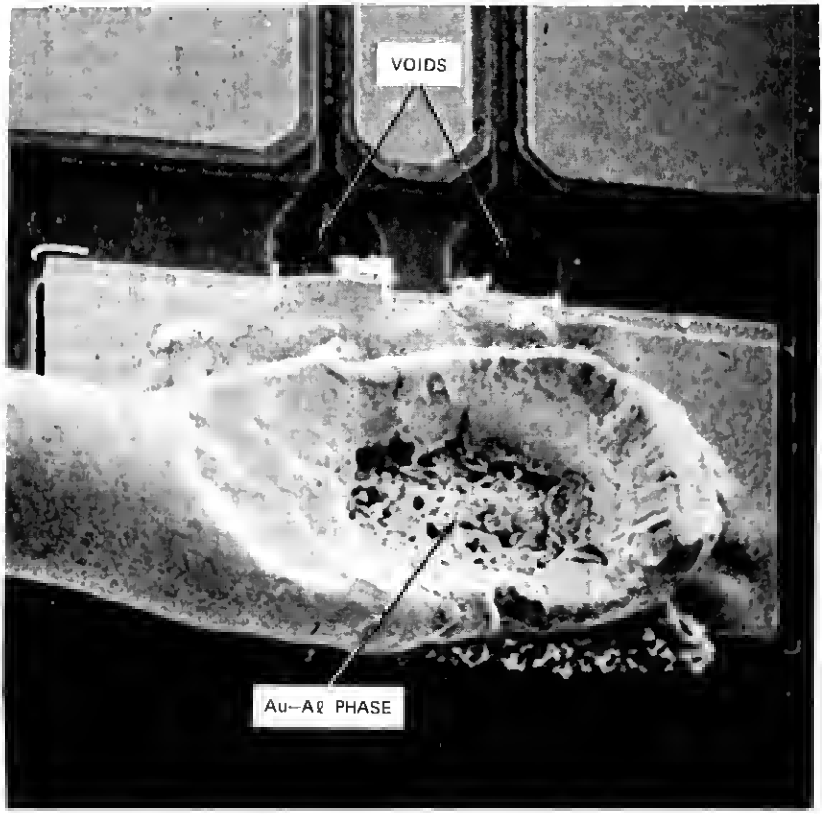

Fig. 4—SEM photo of Au-Al phase at gate-bonding pad of early model FET after aging at 250°C with bias.

as does Si in the case of Si devices[3] (or other devices with SiO_2 layers). Figures 5 and 6 show other examples of Au-Al interaction leading to open gates. Note that the FETs of Figs. 5 and 6 employ the layout shown in Fig. 2, in which the gate bonding pad is separated laterally from the Al structure. However, Au and Al still were able to interdiffuse due to a slight mask misalignment. Both the devices shown in Figs. 4 and 5 were

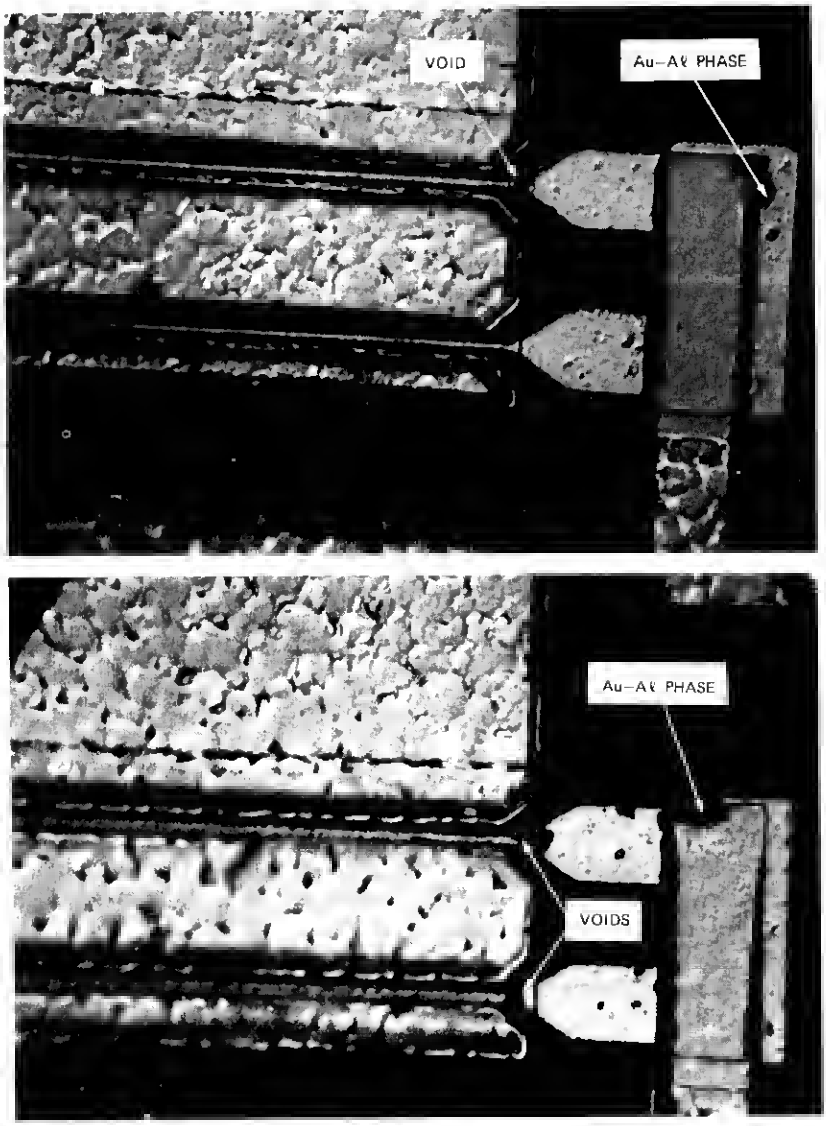

Fig. 5—Optical photos of Au-Al phase and consequent open gates in later model FETs after aging 144 hours at 250°C with bias.

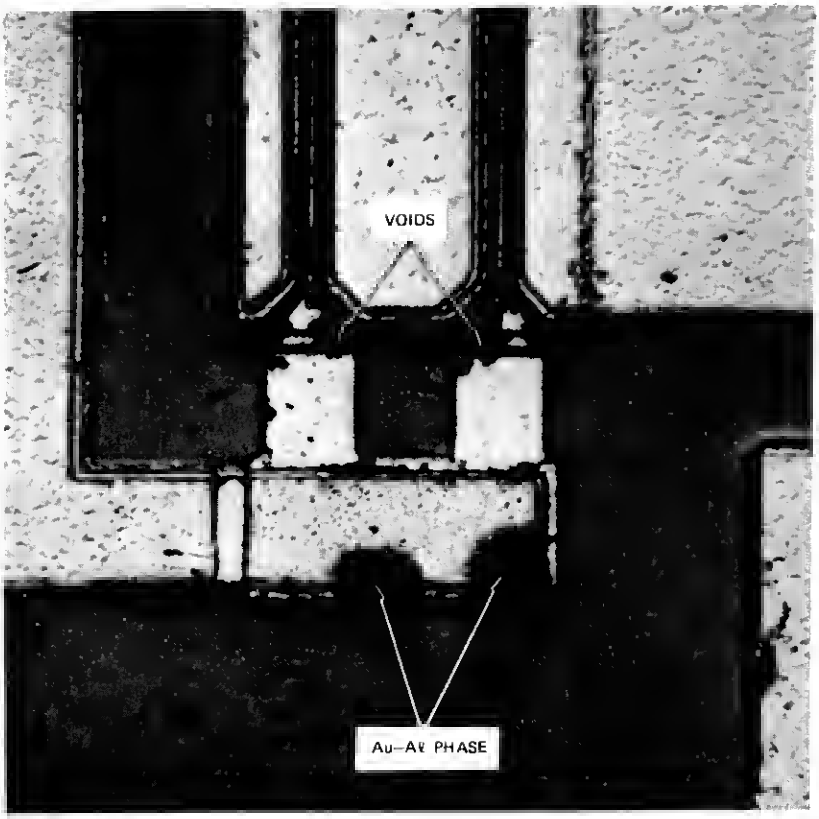

Fig. 6—Optical photo of Au-Al phase and consequent open gates in later model FET after aging at 144 hours at 250°C without bias. (This device is from a slice much more prone to Au-Al phase formation than the device of Fig. 5.)

aged under bias. The FET of Fig. 6 was aged at the same temperature (250°C) without bias.*

The detailed processes of this failure mechanism have not been fully unravelled, but a number of pertinent observations are summarized below.†

(*i*) Every FET that has failed due to an open gate (more than 100 have been examined) exhibits a Au-Al interaction site somewhere in the region where Au and Al overlap. This site may appear to be insignificantly small.

(*ii*) The median time to failure due to open gates is 3 to 10 times longer

* Even with perfect registration, Au-Al contact is expected to occur eventually due to diffusion through the Ti-Pt barrier, though no such cases have been observed so far in these experiments. A mask modification which eliminates the Au layer from the bridge between bonding pad and gate virtually prevents any Au-Al reaction.

† The authors are indebted to A. T. English for his assistance in analyzing the interdiffused gate structures.

among units aged without bias than among identical devices aged at the same temperature with bias.

(*iii*) In all bias-aged failures, a void appears in the gate stripe just where it broadens. This is the point of maximum current density in the gate metallization. Voids may also (but do not always) appear in the broad Al area or at the mesa step.

(*iv*) Failures among units aged without bias have voids scattered generally about the broad Al regions and frequently over the mesa step, but usually not at the aforementioned point of maximum current density.

It is apparent from these observations that there is a decided dependence on the presence of bias. It is important to note that, at 250°C, gate leakage currents at operating bias are one to two orders of magnitude larger than at room temperature, i.e., 20 to 200 μA instead of 1 to 5 μA. Even so, the maximum gate current densities during bias aging are calculated to be only 1×10^4 A/cm^2. This value is generally considered "safe" with regard to electromigration at 250°C. Furthermore, no correlation is found between failure and the gate currents of individual units during aging. Thermal dissipation in biased units in 250°C ambient raises the channel temperature to approximately 258°C. However, unbiased units in 275°C ambient have a much lower incidence of open gates than the 258°C bias-aged units. Thus, this aspect of self-heating cannot explain the bias dependence. Also, joule self-heating within the gate stripe itself is calculated to cause less than 1°C temperature rise, which, of course, also fails to justify much electromigration at these apparently modest current densities. However, current densities in the gate structure are not accurately calculable, since actual Al cross sections vary with the topography of the surface, especially at the mesa edge. It is known that electromigration is influenced by grain size and very little of the voluminous electromigration literature treats stripe widths as small as the 1-μm gates involved here. Thus, electromigration in conjunction with Au-Al phase formation is tentatively thought to be responsible for gate failures in bias aging. Electromigration would transport Al down the stripe away from the bonding pad while Au-Al phase formation causes diffusion in the opposite sense. Perhaps electromigration inhibits Al atoms near the gate throat from replacing the atoms just downstream in the wider portion of the structure (where the current density is less) which are being drawn by diffusion toward the Au-Al compound. The formation of voids may be accelerated by this tug-of-war situation.

If the above hypotheses regarding this gate failure mechanism are correct, the temperature dependence would be quite complex. The activation energy of Au-Al phase formation has been variously reported with values between 0.6 and 1.0 eV.[4] (In any case, the interaction with Ga may alter these values.) Al electromigration (at constant current

density) is reported to have an activation energy of 0.5 to 0.7 eV.[5] However, as mentioned earlier, the gate leakage current itself is temperature-sensitive. The latter two effects together, it is calculated, should give the electromigration an effective activation energy of 1.2 eV.

The experimental situation, unfortunately, is not much clearer. On slices (of the type in Fig. 2) where Au-Al phase formation occurs, its occurrence is quite erratic, depending as it does on slight vagaries in alignment, lift-off, etching, and other details of pattern formation. Thus, among devices aged *without bias*, the median life (ML) varies greatly from slice to slice, though the activation energy observed is fairly consistent and near 1 eV. Electromigration varies as the second or third power of current density which, in turn, differs widely from one unit to another. However, no failures have been observed which appeared to be due to electromigration alone. When units are aged *under bias* at elevated temperature, both mechanisms are thought to be operative, though the degree of dominance by the one mechanism or the other probably varies both among devices and as a function of time during the course of void formation. Initially, phase formation is probably dominant, but when the cross-sectional area has been diminished enough and the local current density increases, electromigration becomes more important. In principle, it is inappropriate to use an activation energy to characterize this joint process consisting of two mechanisms. However, since both mechanisms are expected in this case to have an activation energy near 1 eV, as described above, it is a useful approximation to apply an "activation energy" to the combined effect. As expected, the experimental data are not entirely consistent, but are grouped about a value of 1.0 eV.

No typical ML can be cited for bias-aged devices, since many slices are entirely free of this mechanism. However, in the worst case, an ML of 94 hours at 250°C with bias has been observed. It is important to note that this mechanism has been observed in the present study in devices bias-aged at temperatures as low as 180°C in times as short as 240 hours. Weaver and Brown detected Au-Al interdiffusion at 84°C in 3 hours.[6] Thus, Au-Al phase formation and subsequent destruction of GaAs FETs in which the choice of metallurgy and layout permits this combination cannot be dismissed as an exclusively high temperature phenomenon. However, an appropriate layout can completely eliminate the possibility of Au-Al phase formation.

4.2 Electrolytic corrosion

Figure 7 is an example of electrolytic gate corrosion. The corrosion shown was produced by a 2-hour exposure to an atmosphere of 85°C/85% RH with 6 V negative bias on the gate. The device was uncapped. This corrosion is clearly electrolytic, since in the absence of gate bias no sig-

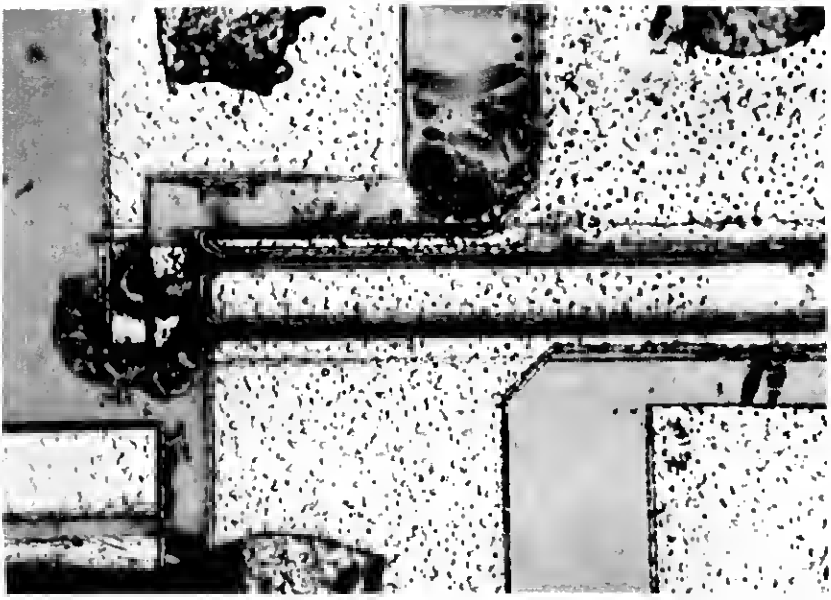

Fig. 7—Optical photograph of FET after 48 hours of aging, uncapped, in 85°C/85% RH humidity chamber, showing electrolytic corrosion of gate.

nificant corrosion is observed. Electrolytic corrosion of unprotected Al structures is well known, of course, from reliability studies of silicon devices.[7] The unusually close electrode spacing and consequent high fields in GaAs FETs as well as the minuteness of the Al gates make them prime candidates for this failure mechanism, in humid conditions. The acceleration factors relative to both varying humidity and temperature have already been reported in the Si device literature[8,9] and is summarized in Section VI.

Various passivation or protective coatings have been proposed for the prevention of electrolytic corrosion in GaAs FETs. Schemes that only coat the GaAs, such as grown oxides, would not be expected to be effective. The highly irregular topography of GaAs FETs complicates the task of achieving a continuous, impervious, pinhole-free, protective film. Equally important is the requirement that the film have small dielectric constant and low microwave loss; otherwise, the sacrifice in microwave performance is unacceptable. None of the films explored in this study fulfills all these specifications perfectly.

A hermetically sealed package can provide permanent protection against electrolytic corrosion from external humidity and without any sacrifice in RF performance, at least at frequencies where a package can be tolerated. It is suspected, however, as observed already among Si devices,[10] that residual impurities entrapped inside the package can produce destructive electrolytic corrosion, although the seal remains

intact. Water and chlorine are the chief offenders, and the trace amount of both which may be adsorbed on the package interior surface are apparently sufficient to produce corrosion. Patches of unremoved photoresist may also harbor enough impurities to cause corrosion. Figure 8 shows the corroded gate of a sealed device that failed after 240 hours under bias in 85/85 though no leak was detectable after removal from the chamber. A Krypton 85 radio-tracer technique was used for leak detection, which has a sensitivity in this case of 10^{-8} std cm^3/s. Though a leak below the detectable limit cannot be excluded and might have caused the corrosion, the Si experience[10] must be borne in mind and residual contamination suspected. This would be confirmed by the discovery of electrolytic corrosion in sealed devices aged at 80° to 90°C in dry air. Among the relatively few devices (30) aged in this manner in the present study, no corrosion has been observed. However, among a group of devices which had failed optical inspection due to unusually

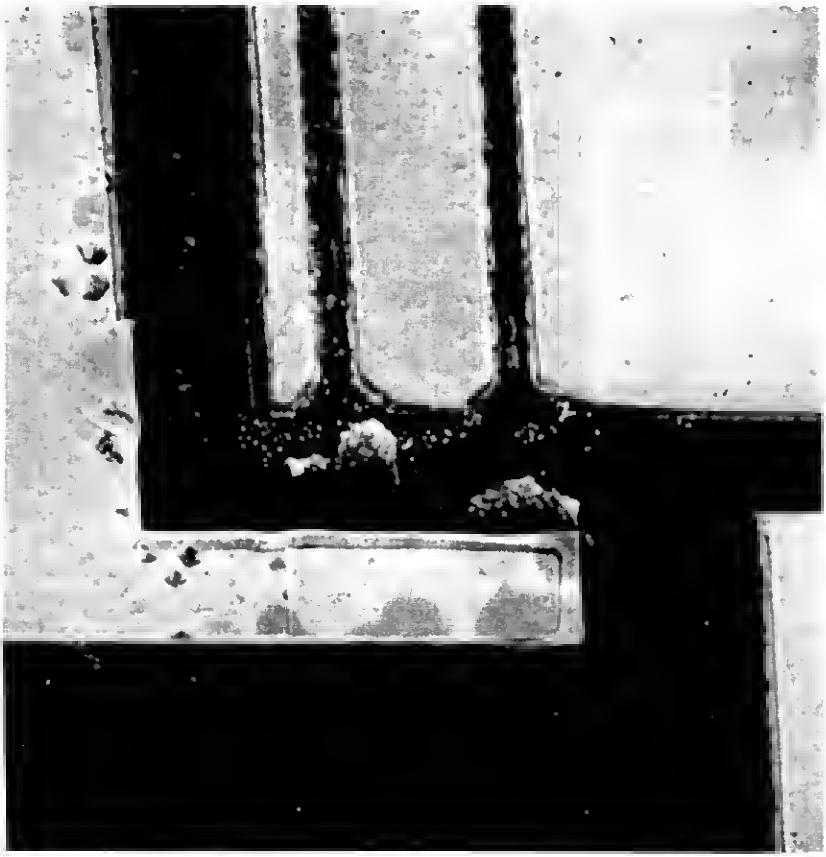

Fig. 8—SEM photograph of corroded gate of FET after 1816 hours of aging, sealed and leak-tight, in humidity chamber. Analysis reveals traces of Cl at corrosion site.

large amounts of photoresist remaining on the chip and which were sealed and aged in 85/85, the incidence of corroded gates was 50 percent in 2000 hours. Altogether, the incidence of electrolytic gate corrosion among "clean" devices which passed optical inspection and which also passed the leak test before and after aging has been about 1 percent in 2000 hours.

V. GRADUAL DEGRADATION MECHANISMS

5.1 High-temperature effects

One of the earliest GaAs FET degradation mechanisms to be discussed was an increase in contact resistance.[11] According to well supported models,[12,13] Ga diffuses out of the crystal into the contact metallization at elevated temperatures. The resulting Ga vacancies probably act as acceptors, compensating the donors in the n-type lamina immediately adjacent to the contact, and thereby increase the contact resistance. The capacity of the metallization for absorbing Ga, or the effectiveness of an interposed barrier to the transport of the Ga, speed or inbibit the degradation process, respectively. In the ohmic contact structure described in Section II and illustrated in Fig. 3, the heavy final gold layer is the largest potential sink for migrating Ga, while the Ag and Ti-Pt layers act as an impeding barrier. As will be seen, however, other factors (such as tbe alloying cycle) must also play a role in the degradation of ohmic contacts.

By means of special test patterns and an appropriate computer program, the contact resistivity, ρ_c, and the channel resistance of a gateless device, $R(ch)$, were measured on certain FET slices before and after aging at 250°C, both with and without bias (0.3 A/cm, the same current per unit source width as in an operating device). A number of actual FETs from the same slice were also aged at the same temperature, with and without bias, and the usual parameters measured (R_S, I_{DSS}, NF, and G). Some slices (which will be designated Class I) showed virtually no change in any parameters after 500 hours, with or without bias, in either test patterns or actual FETs. Other slices (designated Class II), though nominally identical to Class I in design and fabrication, showed startling changes in certain dc parameters, as summarized for one slice in Table I. Typical values of R_S for unaged FETs were 15 to 30 ohms, of which the contact resistance contribution is only 0.2 to 0.5 ohms. The remainder

Table I — Changes in various parameters after 500 hours of aging at 250°C for a Class II slice

	Test Patterns		Actual FETs			
	ρ_c	$R(ch)$	R_S	I_{DSS}	NF	G
With bias	+5000%	0	+50%	−16%	0	0
Without bias	+5000%	0	+20%	−5%	0	0

of R_S is the resistance of the channel and of the semiconductor portions of the source and drain regions. Thus, it would appear plausible that a 5000-percent increase in contact resistance, as shown in Table I, would cause an approximate doubling of R_S. However, it is noted that the change in ρ_c was not affected by bias, whereas the change in R_S and I_{DSS} was very much bias dependent. (The latter bias dependence is also seen in Fig. 9.) The change in R_S (and corresponding change in I_{DSS}) is therefore not wholly attributable to contact deterioration.

The origin of the bias-dependent component of R_S has not been determined. One possibility is recombination enhanced defect formation,[14] though the hole production at the drain and under the gate seems too small for this effect. It is also suggested that the bias-dependent degradation may be related to the gate, since the test patterns, which were unaffected by bias, have no gates. It is also not understood what the essential difference is between Class I and Class II slices—and the continuous spectrum of behavior between these two extremes. It is thought that the least-controlled processing step may be the contact alloying, which is therefore tentatively blamed for at least a part of the slice-to-slice variation in aging behavior. Fortunately, perhaps because the degraded dc qualities of contacts are capacitively bypassed by RF signals,[15] these wide fluctuations in the degradation of dc parameters are not reflected in the RF performance.

Figure 9 shows the average values of R_S, I_{DSS}, NF, and G for two groups of FETs from the same slice (a Class II slice) aged at 250°C, one group with and the other without bias. Though both the dc and RF characteristics degrade faster with bias than without, it is seen that, while R_S doubles, the noise figure and gain only deteriorate by 0.2 to 0.5 dB. Another example is shown in Fig. 10, where NF and G degrade only 0.2 and 0.3 dB, respectively, while again R_S doubles. (The actual contact resistance increased 50-fold.) Two other interesting cases, both representative of many, are shown in Figs. 11 and 12. The devices of Fig. 11 suffered only negligible changes in R_S, I_{DSS}, and NF after 1300 hours of bias-aging at 250°C, though the gain declined about 0.6 dB. Figure 12 shows the data from a group of devices in which none of the measured dc or RF parameters changed significantly in 1500 hours of bias-aging. The results presented in Figs. 9 through 12 may be summarized as follows:

(*i*) There are significant differences among slices in the way the dc and RF characteristics change upon aging.

(*ii*) Radical deterioration of contact resistance (5000 percent) or of source-drain resistance (100 percent) are accompanied by only minor degradation of RF performance; conversely, NF and G may degrade slightly, even though R_S remains constant.

(*iii*) The median life at 250°C under bias, where failure is defined as

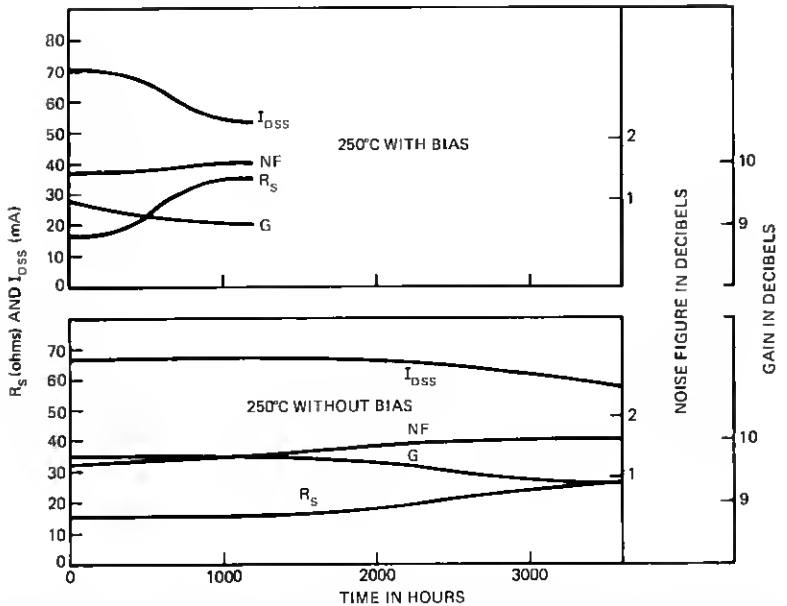

Fig. 9—Plot of median R_S, I_{DSS}, NF, and associated gain as a function of aging time at 250°C for two groups of GaAs FETs from slice (1); Group A aged with bias and Group B aged without bias. (Note acceleration due to bias.)

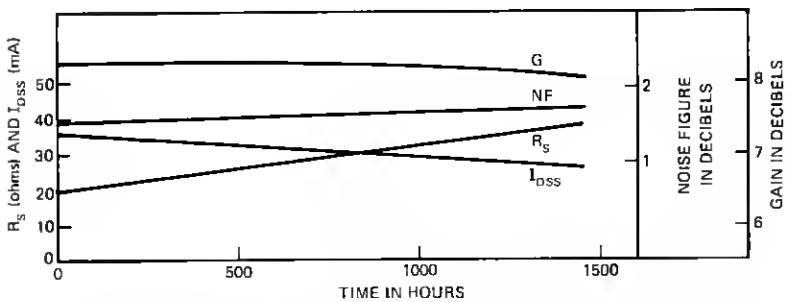

Fig. 10—Plot of median R_S, I_{DSS}, NF, and associated gain of a group of GaAs FETs from slice (2) as a function of aging time at 250°C with bias. (Note NF and G degrade only 0.2 dB, though R_S increases 90 percent.)

an NF or G degradation of equal to or more than 0.2 or 0.8 dB, respectively, is at least 1500 hours.

The observed activation energy of RF degradation is 0.8 to 1.0 eV. It may be noted that many diffusion phenomena within or on the surface of semiconductors, such as might produce traps or scattering centers, have activation energies near 1.0 eV.

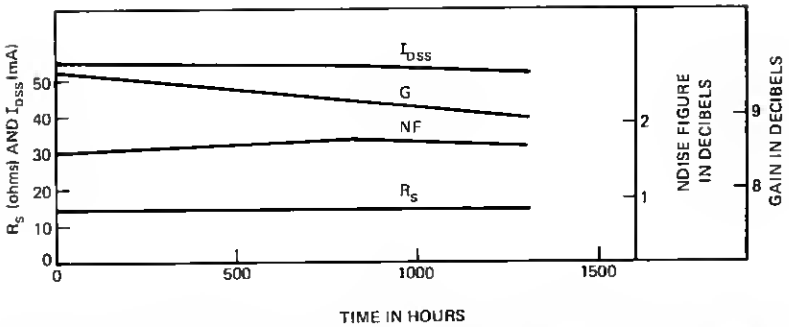

Fig. 11—Plot of median R_S, I_{DSS}, NF, and associated gain of a group of GaAs FETs from slice (3), as a function of aging time at 250°C with bias. (Note NF and G degrade slightly, though R_S in this case remains unchanged.)

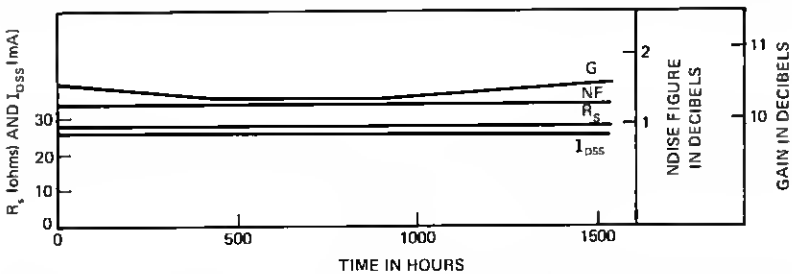

Fig. 12—Plot of median R_S, I_{DSS}, NF, and associated gain of a group of GaAs FETs from slice (4) as a function of aging time at 250°C with bias. (Note that all measured properties remain essentially unchanged.)

VI. FAILURE STATISTICS AND UNOBSERVABLES

6.1 Cumulative failure distributions

The statistics obtained from an aging study depend to some extent upon the definition of failure. A definition of failure can be tailored to a specific failure mechanism and thus he used to sort out data that are relevant exclusively to that mode. Two definitions have been used in various stages of the present investigation.

A. Catastrophic—collapse or radical change in dc output characteristics, usually due to a short or open circuit in one or more of the three electrodes. This definition is especially appropriate for study of the catastrophic mechanisms discussed in Section IV, but ignores any degradation of RF performance not associated with a large change in dc behavior.

B. RF degradation, exclusively—requires that any units that suffer catastrophic failure be subtracted from the population and not counted in the statistics. Figures 9, 10, 11, and 12 were based on such a population. The degree of permitted RF deterioration should be set with system requirements in mind. In this study, unless otherwise specified, a device

was considered to have failed, RF-wise, if the noise figure increased 0.2 dB or more, or the associated gain changed (up or down) by 0.8 dB or more as measured at 4 GHz in a fixed-tuned amplifier.

Figure 13 is a log-normal plot of the cumulative percent failures of type B as a function of aging time for 31 devices representing four separate slices. The aging was performed with bias at 250°C air ambient. The channel temperature is estimated to be 8°C warmer. A few of the devices were sealed, but the majority were not. No difference has been observed in the aging behavior of sealed versus unsealed FETs at this temperature. The data are seen to fit reasonably a straight line, making allowance for the statistical vagaries of small samples, which means they approximate a log-normal distribution. The standard deviation estimate, s, of the line is about 1.3, obtained from the operational calculation

$$s = \ln[t(50)/t(16)],$$

where it is noted the natural logarithm is used and $t(50)$ and $t(16)$ are the times corresponding to 50 and 16 percent cumulative failure, respectively. The median life of this group is about 1700 hours. The results shown in Fig. 13 are typical of the RF degradation observed in this study.

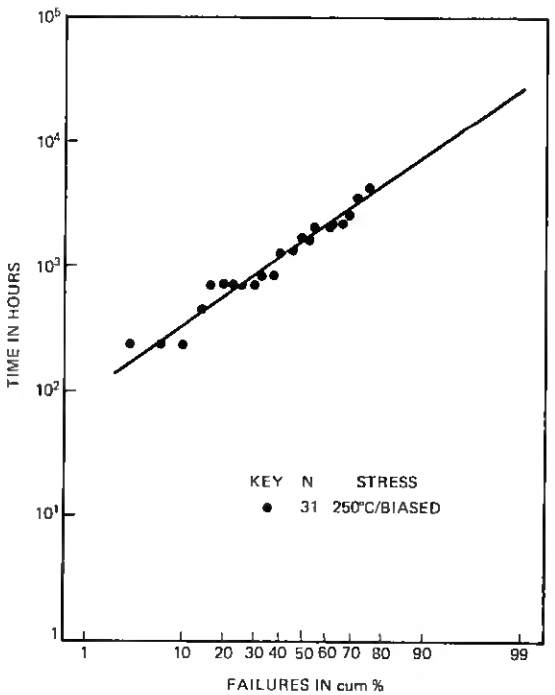

Fig. 13—Log-normal plot of cumulative failure distribution (RF degradation) of a group of GaAs FETs aged with bias at 250°C.

Figure 14 shows the cumulative failure distributions at 250°C of two groups of units from one slice, one aged with bias and the other without bias. The MLs are about 100 hours and 350 hours, respectively, with nearly the same standard deviation of $s = 1$. The failures in this case are all type A and due to Au-Al phase formation, plus an apparent assist from electromigration in the biased group, as discussed in Section 4.1. This slice was unusually susceptible to the Au-Al phase problem and is chosen here to illustrate the failure statistics of that mechanism.

6.2 Humidity acceleration factors

Electrolytic corrosion is accelerated by increased humidity and temperature mainly as a result of and in proportion to the increased electrical conductivity of the surface. The problem has been most recently studied by Sbar and Kozakiewicz,[9] who give acceleration factors with respect to 85°C/85% RH for various encapsulations and temperature/humidity conditions. Though the absolute value of conductance on a GaAs surface may differ from that on a Si, Si_3N_4, or alumina surface, the temperature and humidity dependence are expected to be similar. For 60°C/5% RH (a choice which will be justified later), the Sbar-Kozakiewicz results indicate an acceleration factor of 2×10^5 with respect to 85/85. For a condition of 60°C/25% RH, the factor is about 10^4. Both values apply to an unencapsulated device. For a perfectly sealed device, of course, the external humidity has no effect. The only acceleration of electrolytic

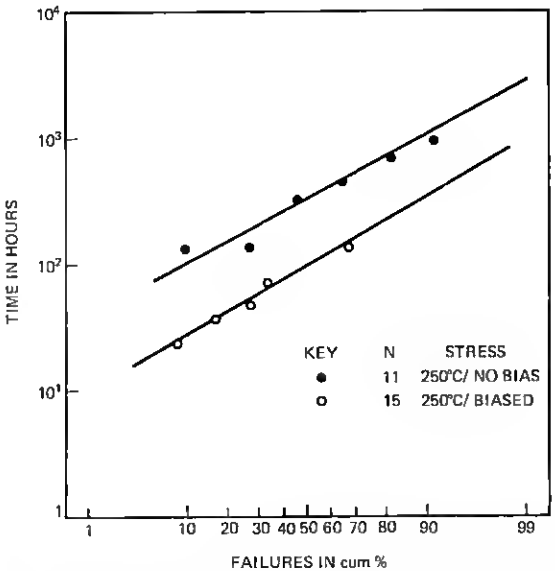

Fig. 14—Log-normal plot of cumulative failure distributions of two groups of GaAs FETs aged at 250°C with and without bias. (All failures were due to gate destruction by Au-Al phase formation plus, in one case, a bias-dependent factor.)

corrosion would be that due to the temperature elevation, assuming there are sufficient contaminants inside the package to produce an electrolyte, but that their release is not temperature-sensitive. The acceleration factor at 85°C relative to 60°C is approximately 3.

6.3 Statistical error

During the course of this study, numerous small changes have been made in the design or fabricational methods of the device under investigation. Since it was desirable to appraise the reliability aspects of each of these variations and both facilities and device are limited in supply, the strategy has been to age many small lots of FETs rather than fewer and larger lots. The relatively small sample size (10 to 20) raises questions about the validity of the statistics obtained. It should be pointed out, therefore, that with a sample size of 10, one can be 90 percent confident that the true ML (i.e., the ML of an infinitely large sample) would be somewhere between 45 and 225 percent of the observed value, assuming a log-normal distribution with a standard deviation of 1. Thus, in the next section where failure rates are calculated, error tolerances may be attached to the values given by noting that in the area where most of the data fall, a factor of 2 in ML produces a factor of approximately 2 to 3 in failure rate.

6.4 Possibility of unobserved failure mechanisms

A relatively small number of FETs have been aged under bias for periods of 0.5 to 1.5 years at moderate or room temperatures (more precisely, 30 units at 180°C for 6000 hours, 10 units at 88°C for 4600 hours, and 30 units at 27°C for 8000 to 14,000 hours, all in air ambient). Judging from the statistics obtained at higher temperatures, provided that only the same mechanisms prevail, no failures or degradation should be apparent in these modest times at lower temperature, except possibly for the Au-Al phase-migration problem. Indeed, this turns out to be the case: five units of one lot of 10 at 180°C have failed due to the Au-Al syndrome, but otherwise no degradation appears in any of the units.

The lack of any failures among the other units provides some lower bound to the activation energy of any failure mechanism which may be important at lower temperature but is obscured at higher temperatures by phenomena with higher activation energies. (This sort of insidious situation has been encountered in Pt-GaAs IMPATTs.[16]) It will be assumed that such a failure mechanism would have a log-normal failure distribution with a standard deviation of 1. It is noted furthermore that the absence of a single failure in a lot of 30 indicates with 90 percent confidence that the true percent failure cannot exceed 10 percent. Finally, it is noted that the ML of any such so-far-unobserved failure mechanism must be at least 1700 hours at 250°C, since that is the longest

observed ML at that temperature due to recognized mechanisms. Combining these arguments leads to the conclusion that the minimum activation energy of a failure mechanism active at 180°C, but obscured at 250°C is 0.7 eV. However, the minimum activation energy for a failure mechanism dominant at 27° to 180°C but not yet observed in this program is only 0.03 eV. The latter figure is rather alarming. It means, in conjunction with the high temperature data, that if such a hypothetical mechanism exists, the projected ML at room temperature would be 30,000 hours and the ML would be only negligibly accelerated by elevated temperatures. The duration of the present reliability program is insufficient to rule out such a possibility. However, it is reassuring that other investigators have reported room temperature tests of low-noise GaAs FETs of similar metallurgy in excess of six years without any failures.[17]

6.5 Infant mortality

Few instances of infant mortality have been found in this study. There are two reasons: (*i*) rigorous optical inspection of all chips before mounting and discarding of any units which appear mechanically or electrically defective after mounting eliminate most devices that might otherwise be candidates for early failure; (*ii*) the small size of the samples used further diminishes the probability of encountering anomalous devices representing only a small proportion of the population. Thus, this work sheds no light on the nature of such early failures except that, with the present fabrication, inspection, and testing procedures, their occurrence is less than 1 percent. The failure and degradation mechanisms discussed here and the failure rates projected pertain to the main body of the population. It must be anticipated that some cases of infant mortality will accompany large-scale production and deployment of this device.

VII. ESTIMATION OF FAILURE RATES

Given the nature of the failure distributions at an elevated temperature and their respective activation energies, and making the all-important assumption that the mechanisms studied at elevated temperature are also the dominant ones at room temperature, and with the further assumption that the nature of each failure distribution is not temperature-dependent (i.e., it stays log-normal with the same s), it remains only to specify the operating conditions in order to calculate the probable failure rates in the field. The maximum ambient temperature in a Bell System radio relay application is 52°C (125°F). The corresponding maximum channel temperature would be 60°C. Though the annual average temperature would certainly be considerably lower, 60°C will be taken as the channel temperature for calculation of failure rates. Three separate cases will be considered.

7.1 Case I: No catastrophic mechanisms

In this case, it is assumed all fabricational steps have been faultless, assuring the absence of any contact between Au and Al, a contamination-free chip and package interior, and a leak-tight seal. The catastrophic failure mechanisms are therefore precluded, and only long-term degradation of RF properties is of concern. The median lifetime (type B) at 258°C was found to be about 1700 hours, and the associated activation energy will be taken as 0.8 eV. Thus, the projected ML at 60°C would be 4×10^7 hours. Taking a standard deviation of 1.0 and using Goldthwaite's curves,[18] the failure rate after 20 years of service is found to be less tban 10^{-2} FIT (1 FIT = 1 failure in 10^9 device-hours). It should be noted that, with a standard deviation of 1.5, the projected failure rate would be 2 FITs and with $s = 2$, the failure rate is 30 FITs, i.e., the difference between $s = 1$ and $s = 2$ is more than 3 orders of magnitude in failure rate. Thus, an accurate knowledge of the standard deviation is vital to the accurate forecasting of failure rates. However, the low confidence levels of the statistics do not justify quibbling over the real value of s, and the predicted failure rates are small in any case (but do not include infant mortality).

7.2 Case II: Au-Al phase formation dominant

As mentioned in Section 4.1, the ML due to Au-Al phase formation at 250°C has been observed to be as short as 94 hours, though it exceeds observation times in many cases. Based on this shortest observed ML and the smallest observed activation energy of 0.5 eV, a worst-case prediction is obtained, indicating that for an unscreened product the failure rate could go over 10,000 FITs, i.e., 1 percent per 1000 device-hours. However, a reliability qualification test of each slice can be used to assure that the ML due to the Au-Al/electromigration syndrome is no less than 500 hours at 250°C. Assuming a relatively conservative value of 0.8 eV for the activation energy (from the wide range observed of 0.5 to 1.6 eV), an ML at 60°C of 1×10^7 hours is projected. Taking $s = 1$, as found in Fig. 14, gives an estimated failure rate of 0.6 FIT in a 20-year service period. Taking $s = 1.5$, as found in occasional slices also dominated by the Au-Al failure mechanism, gives a failure prediction of 40 FITs. The latter value is considered a realistic upper limit for devices of the type shown in Fig. 2 subjected to a reliability screening procedure (and is therefore the value quoted in the abstract).

7.3 Case III: Electrolytic corrosion dominant

If unsealed, unprotected low-noise GaAs FET chips were employed in an amplifier in which the housing was not hermetically sealed, electrolytic corrosion as described in Section 4.2 would be expected. Since in some radio relay applications, the waveguide is pressurized with 5-

percent RH air, this value for the ambient will be considered for the first example. (It should be noted that 30°C/25% RH air becomes 5% RH air when heated, at constant water vapor content, to 60°C). For unprotected units in 85/85, an ML of about 3.5 hours due to electrolytic corrosion has been observed. Using the appropriate acceleration factor of 2×10^5, as described in Section 6.2, an ML of 7×10^5 hours at 60°C/5% RH is predicted. The corresponding failure rate is about 1000 FITs. For a second example, an atmosphere of 60°C/25% RH is chosen, which may be obtained by heating 32°C (90°F)/100% RH air up to 60°C. In this case, an ML of 3.5×10^4 hours and a failure rate of about 20,000 FITs after 5 years are predicted.

As a third example, it might be assumed that the GaAs FET chip is unprotected and the amplifier is hermetically sealed, but not adequately free of contaminants. Indeed, in view of the large amount of surface within an amplifier and the difficulty of giving it a high-temperature vacuum bakeout, it very likely would contain dangerous amounts of residual impurities. An ML of about 2000 hours has been observed in this study with contaminated packages at 85°C. The acceleration factor relative to 60°C in this case is only 3, as discussed in Section 6.2. Thus, an ML of 6000 hours might be anticipated for this amplifier with unsealed, unprotected FETs and a first-year failure rate of over 50,000 FITs.

It is emphasized that the above three examples of electrolytic corrosion assume unsealed, unprotected (unpassivated) devices. In the case of a clean, hermetically sealed device, electrolytic corrosion is effectively prevented, and no failures due to that mechanism are expected.

VIII. CONCLUSIONS

Two catastrophic failure mechanisms were found in this study of low-noise GaAs FETs, not including voltage transients which are considered primarily a problem of handling technique and circuit design. One of these mechanisms is Au-Al phase formation occurring at the junction of the Al gate and its Au bonding pad. This mechanism is enhanced by bias through what appears to be electromigration, though positive evidence of the latter is lacking. In a worst case, this mechanism could give rise to failure rates as high as 10,000 FITs, though with appropriate slice screening, values in the neighborhood of 1 to 50 FITs appear more likely. Proper design and fabrication methods can eliminate this mechanism entirely. The other catastrophic failure mechanism is electrolytic corrosion of the Al. In a humid environment or in a contaminated package, failure rates again in the order of 10,000 FITs might be anticipated. However, hermetic sealing in a contaminant-free package eliminates this problem. It is noted that both these failure mechanisms are related to the choice of an Al gate. They are not peculiar to GaAs FETs, but are well known as causes of failure in Si devices.

In the absence of catastrophic failure, a long-term, gradual degradation of noise figure and gain is observed. This effect is only weakly correlated with increase of contact resistance and is apparently more strongly influenced by other factors such as the formation of traps and scattering centers. The median lifetime due to this gradual RF degradation is estimated to be over 10^7 hours at a channel temperature of 60°C. The corresponding failure rate after 20 years of service is less than 2 FITs.

All the important failure modes were accelerated by the presence of drain and gate bias. Aging without bias would give erroneously optimistic predictions.

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